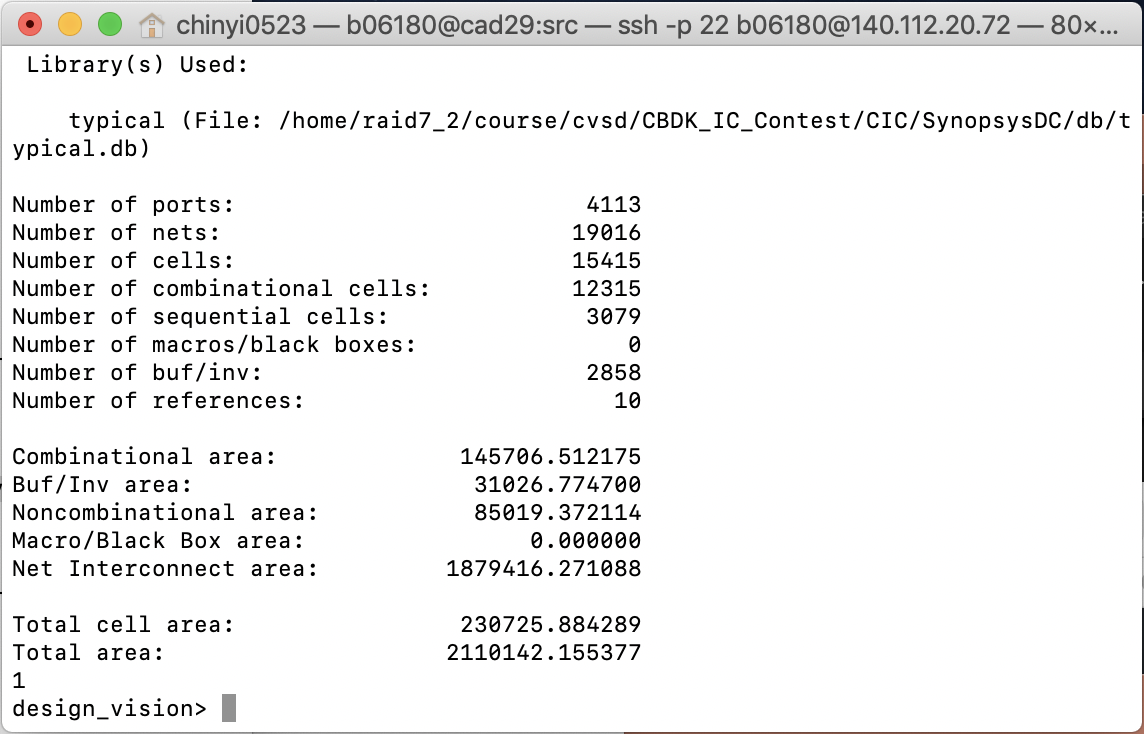
**DSD Final Project Scores (RISC-V)**

**1. Baseline**

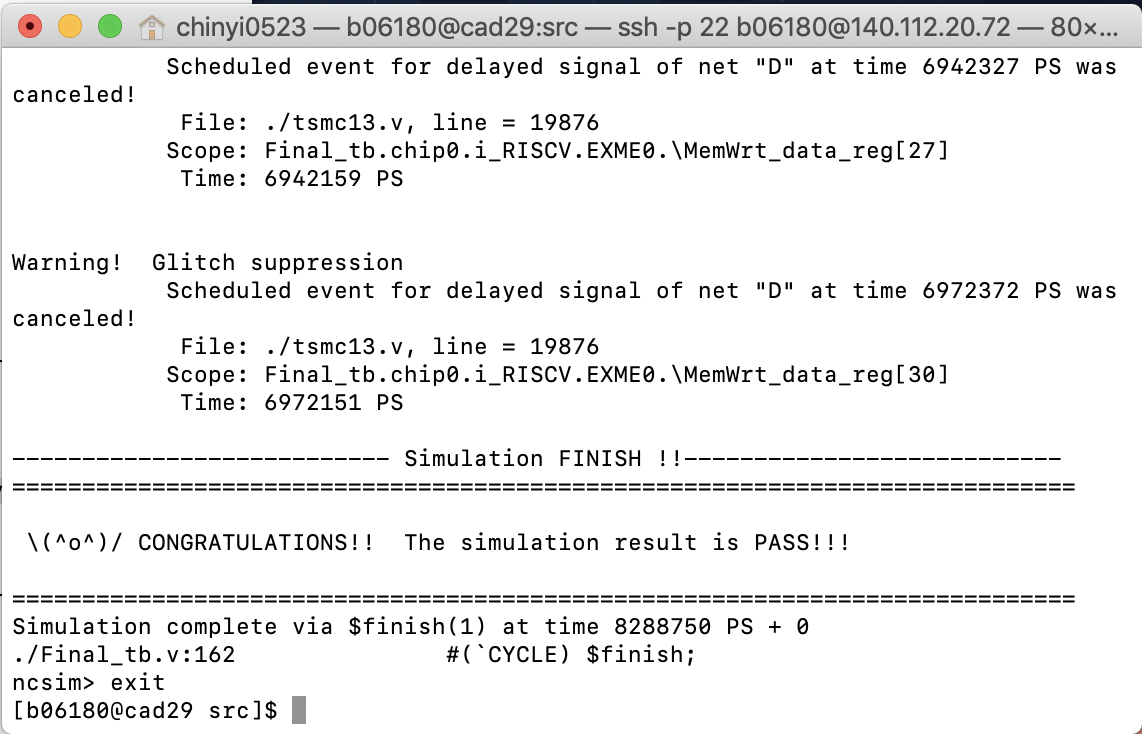
(1) Area: (um2)

截圖:



(2) Total Simulation Time of given hasHazard testbench: (ns)

截圖:



(3) Area\*Total Simulation Time: (um2 \* ns)

1,912,429,173.4004

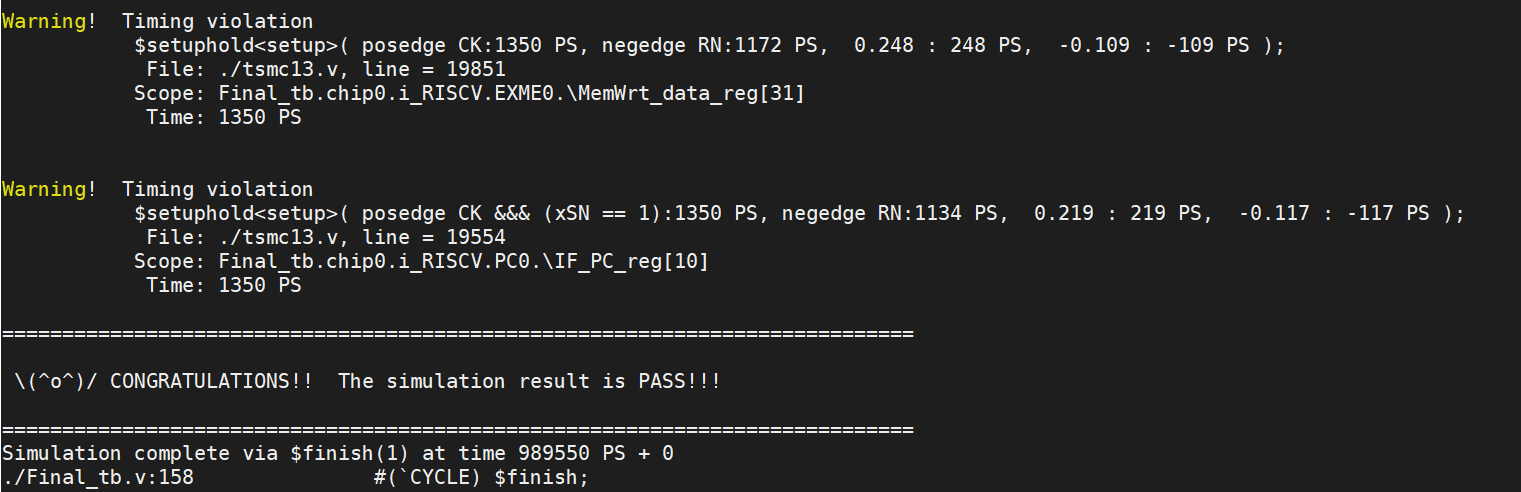
(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

2.6

**2. BrPred**

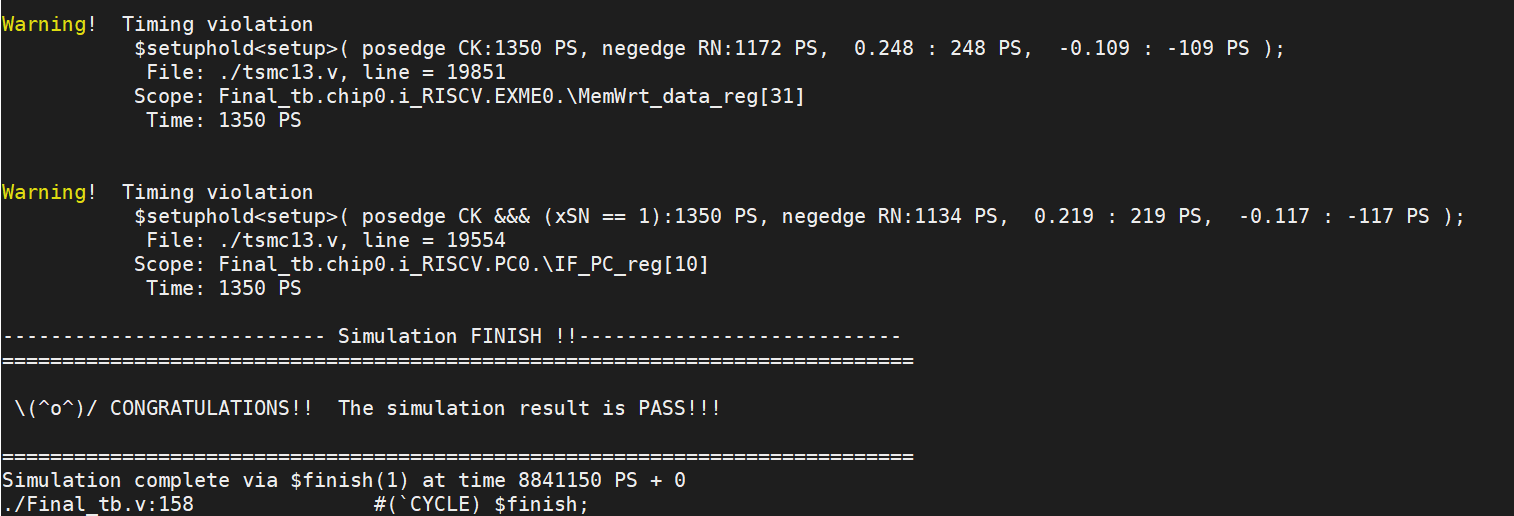
(1) Total execution cycles of given I\_mem\_BrPred:

截圖:



(2) Total execution cycles of given I\_mem\_hasHazard:

截圖:



(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um2)

15042.359113

**3. L2 Cache**

(1) Average memory access time: (ns)

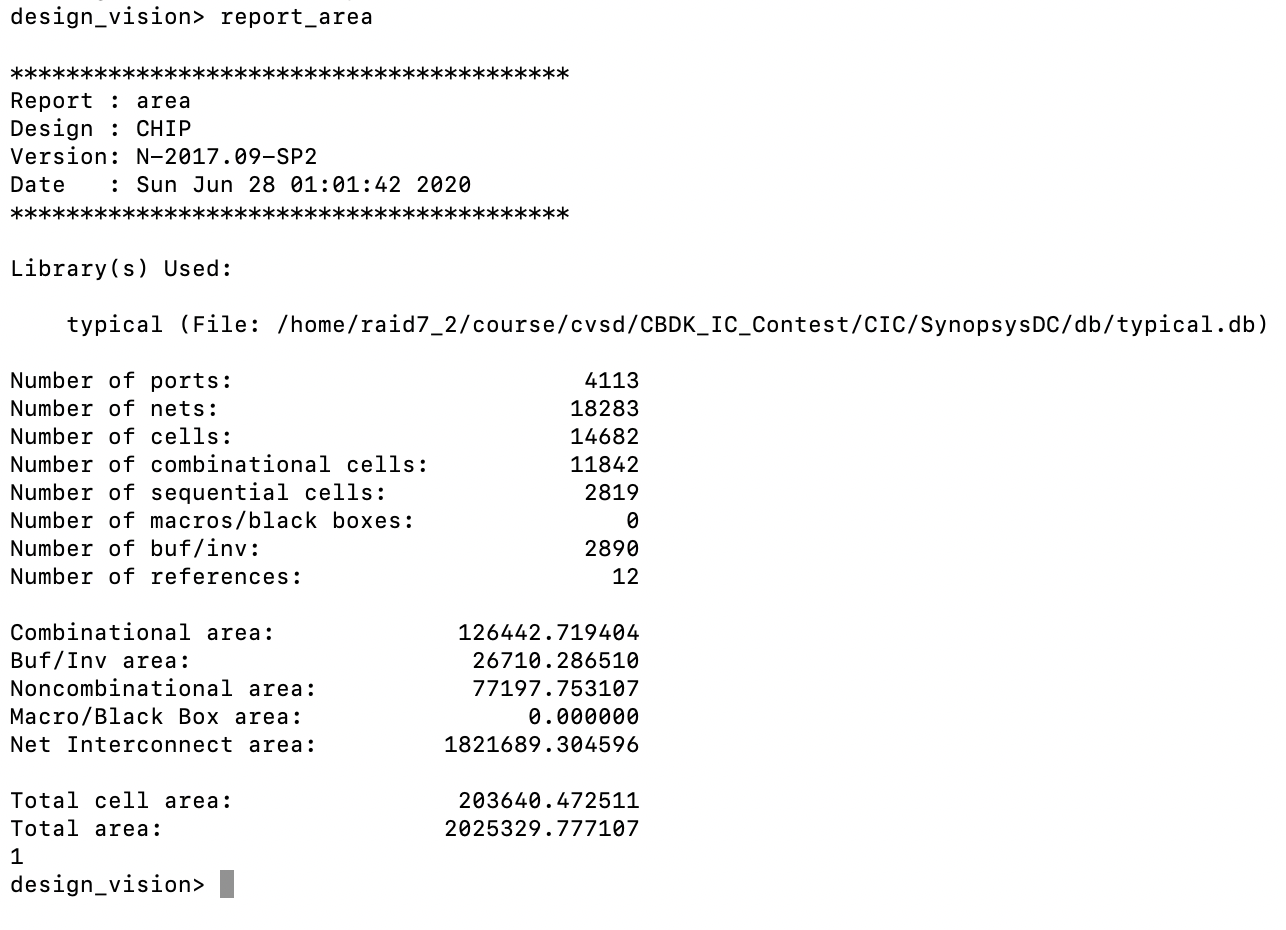
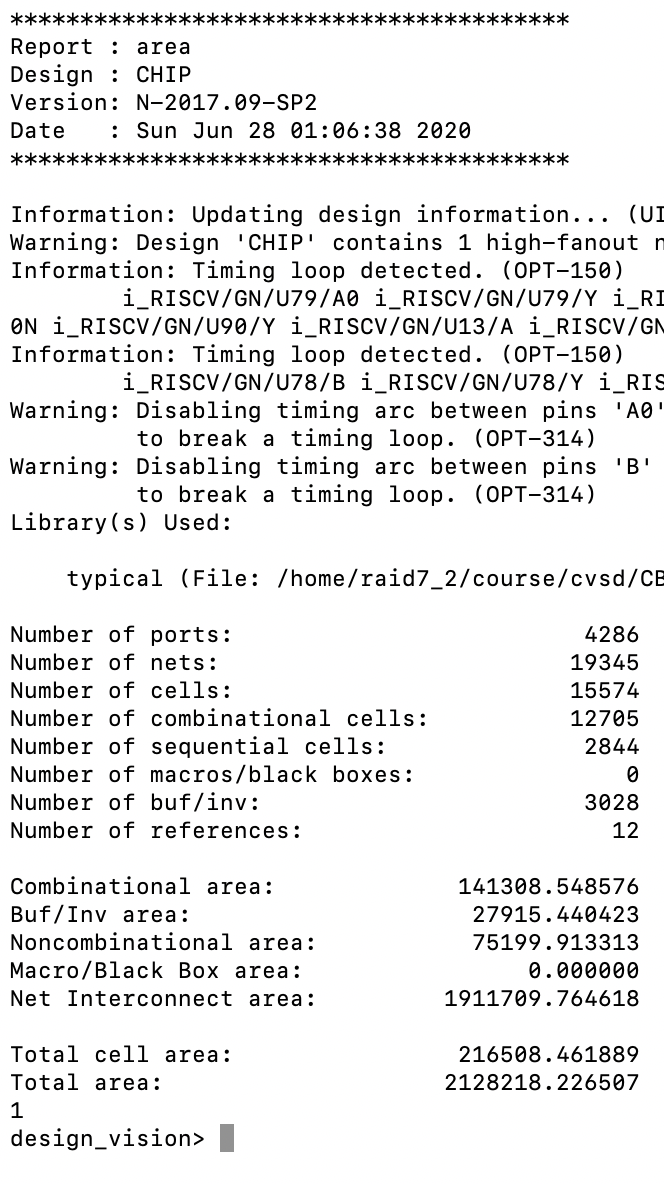
(2) Total execution time of given I\_mem\_L2Cache: (ns)

截圖:

**4. Compressed instructions**

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um2)

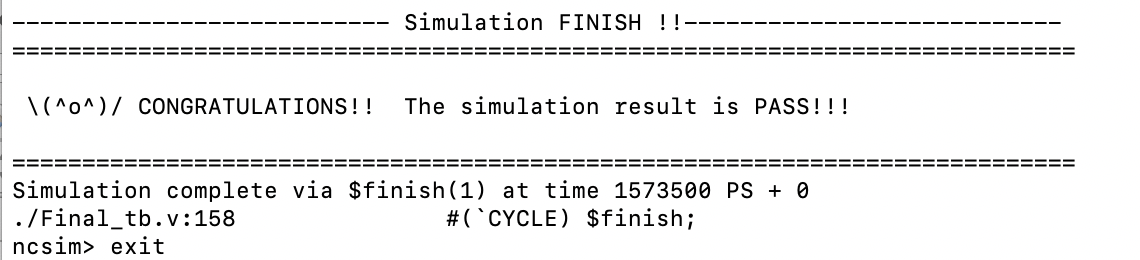
截圖:



216,508.5-203,640.5 = 12,868.0 (um2)

Both of design use non-blocking cache, with synthesis cycle = 3ns.

(2) Total Simulation Time of given I\_mem\_compression: (ns)

截圖:

Simulation Time : 1,573.5 (ns)

(3) Area\*Total Simulation Time: (um2 \* ns)

AT = 340,676,124.8 (um2 \* ns)

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

3 ns